IN THE CLAIMS

Please amend the claims as follows, substituting any amended claim(s) for the corresponding pending claim(s):

1. (Previously Presented) A wireless transceiver device, comprising:

modulation circuitry for modulating and demodulating signals that are transmitted over airwaves;

frequency conversion circuitry for up converting and down converting between radio frequency signals and baseband frequency signals;

digital-to-analog conversion circuitry for converting from analog to digital and from digital to analog;

a radio controller;

baseband processing circuitry including a first in, first out (FIFO) memory structure for storing addresses for accessing data blocks; and

a plurality of command blocks formed within a memory structure, the command blocks include addresses of data blocks stored within random access memory and a memory portion for storing an indicator for indicating whether a command block of the plurality of command blocks is in use.

Claim 2. (Cancelled)

3. (Previously Presented) The wireless transceiver device of claim 1 wherein the FIFO memory structure includes pointers that define addresses of the command blocks.

Claim 4. (Cancelled)

5. (Previously Presented) The wireless transceiver device of claim 1 wherein the modulation circuitry includes Gaussian Phase Shift Keying modulation and demodulation circuitry.

6. (Previously Presented) The wireless transceiver device of claim 1 wherein the frequency conversion circuitry converts directly between radio frequency and baseband.

7. (Previously Presented) A method for storing and transmitting data, comprising:

storing a data block in random access memory; and

storing a pointer that corresponds to the data block in a first in, first out (FIFO) memory structure, the pointer includes an address of a command block;

storing an address of the data block in the command block; and

setting an indicator signal in a defined memory location, wherein the indicator signal indicates that the data block address stored in the command block is for data that has yet to be successfully transmitted and that the command block is busy.

Claims 8-10. (Cancelled)

11. (Previously Presented) The method of claim 7 wherein an address for a data block is only stored in a command block if the indicator signal reflects that the command block does not contain the address of a data block that has yet to be successfully transmitted.

12. (Previously Presented) The method of claim 7 further comprises:

evaluating the command block address included within the FIFO pointer.

13. (Previously Presented) The method of claim 12 further comprises:

examining the contents of the command block specified by the pointer to determine a data block address.

14. (Previously Presented) The method of claim 13 further comprises:

evaluating at least a first memory location of the data block whose address is stored in the command block to determine a data block size.

15. (Previously Presented) The method of claim 14 further comprises:

retrieving an amount of data corresponding to the data block size and transmitting that data to a radio modem for transmission over wireless airwaves.

16. (Previously Presented) The method of claim 15 further comprises:

resetting the indicator signal if the transmission was successful.

17. (Previously Presented) A memory structure formed within a baseband processing system, comprising:

a random access memory portion for storing data blocks that are to be transmitted in a first in, first out (FIFO) order; and a FIFO memory structure for storing pointers that correspond to the data blocks stored in the random access memory portion;

a plurality of command blocks defined within the random access memory portion wherein each command block is for specifying an address of a data block that is to be transmitted; and

a defined memory portion for storing command block indicators for each command block, wherein the command block indicators specify whether its corresponding command block includes the address of a data block that has yet to be transmitted successfully.

Claims 18-19. (Cancelled)

20. (Previously Presented) The memory structure of claim 17 wherein the defined memory portions for storing the command block indicators are each one bit in length.

21. (Previously Presented) The memory structure of claim 17 wherein the command blocks defined within the random access memory portions are each four bytes in length.

22. (Previously Presented) The memory structure of claim 17 wherein the FIFO memory structure defines a plurality of FIFO memory blocks wherein each FIFO memory block relates to data blocks that are to be transmitted to a particular device.